## REMARKS

### Present Status of the Application

Claims 1-13 are pending.

Claims 1-8 are objected to under 37 CFR 1.75(d)(1) because of an improper use of antecedent basis.

Claims 1-13 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, has possession of the claimed invention.

Claims 1-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 3, 7-9, and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawauchi (US 5,619,653), and further in view of Nanba (US 4,665,484) and Fujimoto (US 5,418,913).

Claims 2 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawauchi (US 5,619,653), in view of Nanba (US 4,665,484) and Fujimoto (US 5,418,913), and further in view of Fried et al (US 5,142,676).

Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawauchi (US 5,619,653), in view of Nanba (US 4,665,484) and Fujimoto (US 5,418,913), and further in view of

Balmer et al (US 5,742,599).

**Response to Objections to Claims**

The term "*the message target row*" in the claims is amended to read "*the target message row*" according to the Examiner's advice. Moreover, he phrase "*without permission of the write control unit and the source controller*" is canceled from claim 1, and the phrase "*without permission of the source controller*" is canceled from claim 9. After entry of the foregoing amendments, it is respectfully submitted that the objections to the claims should be withdrawn.

**Response to Claim Rejections Under 35 U.S.C. 103(a)**

In response to the aforesaid rejections, Applicants have amended claims 1 and 9 to describe the claimed invention more explicitly. The feature "*a write control unit, coupled to the source controller and the plurality of message rows*" recited in claim 1 is amended to read "*a write control unit, coupled between the source controller and the plurality of message rows*", and the feature "*a read control unit, coupled to the destination controller and the plurality of message rows*" recited in claim 1 is amended to read "*a read control unit, coupled between the destination controller and the plurality of message rows*". Moreover, the feature "*wherein the plurality of message rows are coupled between the write control unit and the read control unit*" is added into claim 1. The amendments about the connections of the source controller, the write control unit, the plurality of message rows, the read control unit, and the destination controller are supported by FIG. 1 of the present application. Referring to FIG. 1 of the present application, the write control

unit 165 is coupled between the source controller 110 and the plurality of message rows 130, the read control unit 195 is coupled between the destination controller 120 and the plurality of message rows 130, and the plurality of message rows 130 are coupled between the write control unit 165 and the read control unit 195. No new matter is introduced.

Additionally, claims 1 and 9 are amended to include the limitations "*the distribution complete flag of the target message row and the write complete flag of the target message row are set by the write control unit*" and "*the distribution complete flag of the target message row and the write complete flag of the target message row are both cleared by the read control unit*". Supports of the amendments could be found in the specification of the present application. For example, the paragraph [0006] recites that "*when the source controller completes reading the address of the message row, the write control unit sets the distribution complete flag of the message row*" and that "*when the source controller completes writing the message of the message row, the write control unit sets the write complete flag of the message row*", the paragraph [0024] recites that "*when the destination controller completes reading a message row, the read control unit clears the distribution complete flag and the write complete flag of the message row pointed to by the read pointer*". No new matter is introduced.

In addition, the limitation "*a message transmitting queue having a plurality of message rows, a write pointer and a read pointer*" recited in claim 9 is amended to read "*a message transmitting queue having a plurality of message rows, a write control unit and a read control unit*", and the features "*the plurality of message rows are coupled between the write control unit and the read control unit*" and "*the write control unit has a write pointer, and the read control unit*

*has a read pointer*" are added into claim 9. The amendments are supported by the specification and the drawings of the present application. For example, as shown in FIG. 1, the message transmitting queue 100 has the plurality of message rows 130, the write control unit 165 and the read control unit 195. The write control unit 165 has the write pointer 140, and the read control unit 195 has the read pointer 170. The plurality of message rows 130 are coupled between the write control unit 165 and the read control unit 195. No new matter is introduced.

After entry of said amendments, it is respectfully submitted that the pending claims 1-13 are patentably distinguishable over the cited references for at least the following reasons.

As acknowledged by Examiner's Action, Kawauchi fails to teach the use of a distribution complete flag, as recited by claims 1 and 9. To overcome this admitted deficiency, the Action relies on the teachings of Nanba. However, Applicants believe that there is no suggestion or motivation to make the proposed modification **because the proposed modification would render Nanba unsatisfactory for its intended purpose**. Please refer to MPEP § 2143.01, subsection V, which recites "If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification". *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).

As recited in the amended claims 1 and 9 of the present application, the distribution complete flag of the target message row is set ***by the write control unit***, and the distribution complete flag of the target message row is cleared ***by the read control unit***. Referring to FIG. 1 of the present application, a distribution complete flag (C0-C3) of a target message row (130) is set ***by the write control unit 165*** when the source controller (110) reads an address of the target message

row (130), and the distribution complete flag (C0-C3) of the target message row (130) is cleared ***by the read control unit 195*** once the destination controller (120) completes reading the message of the target message row (130). In addition, as shown in FIG. 1 of the present application, the plurality of message rows 130 are coupled between the write control unit 165 and the read control unit 195. Therefore, the distribution complete flag (C0-C3) is cleared by the read control unit 195, which is different from the write control unit 165.

However, Nanba teaches that the lock flag/bit, i.e. the first bit of the GATE, **is set and cleared by the same processor** before the shared resource is released. Firstly, according to the specification of Nanba, the first bit of the GATE is used to indicate whether the shared resource is in a locked status or in an unlocked status. The first bit of the GATE is set to "1" if the shared resource is locked, and the first bit of the GATE is set to "0" if the shared resource is unlocked. Secondly, Nanba teaches that "*At step 68, the processor P0 applies the address signal indicative of the GATE address via the address bus AB, while applying the data having all bits "1"s to the entire GATE ..... The reason that the all logic "1"s are stored in the entire GATE at step 68, is* ***to prevent the other processors from accessing the shared resource which the processor P0 intends to use***" (see col. 4, line 63 to col. 5, line 7) and that "*a program executed on the processor P0 intends to use a shared resource and hence is going to lock same* ***for the exclusive use thereof***" (see col. 4, lines 41-43). Referring to FIG. 2 of Nanba, when the processor P0 uses a shared resource in the main memory 40, the processor P0 sets all bits of the GATE of the shared resource to "1" so as to prevent the other processors P1 and P2 from using the shared resource. Since the other processors P1 and P2 cannot use the shared resource, which is locked by the processor P0, the first bit of the GATE of

the shared resource would not be cleared by the other processors P1 and P2. In other words, if Nanba allows the first bit of the GATE being set to "0", i.e. cleared, by the other processor P1 or P2, the shared resource locked by the processor P0 would be released by the other processor P1 or P2 even if the processor P0 still uses the shared resource. In such case, the processor P0 would fail to lock the shared resource ***for exclusive use thereof***, and the program executed on the processor P0 may operate erroneously due to misplacement or overlap of the shared resource.

For at least the foregoing reasons, the first bit of the GATE of Nanba must be set and cleared by the same processor. Otherwise, Nanba will fail to lock the shared resource to prevent other processor from using the shared resource. Therefore, Applicants believe that the teachings of the references are not sufficient to render the claims 1 and 9 obvious **since the proposed modification would render Nanba unsatisfactory for its intended purpose** (i.e. exclusive use of resource).

Moreover, Examiner suggested that the controller 110 of Kawauchi is equivalent to both ***the write control unit*** and ***the read control unit*** as recited in claim 1 of the present invention. However, the controller 110 of Kawauchi is a single unit rather than two different units. Moreover, as recited in the amended claims 1 and 9, a plurality of message rows are coupled between the write control unit and the read control unit, but Kawauchi fails to disclose such connections. Therefore, the controller 110 of Kawauchi is not equivalent to the write control unit and the read control unit of the present invention.

For at least the above reasons, independent claims 1 and 9 of the present application are not obvious over the cited references. It is respectfully submitted that independent claims 1 and 9 and

their dependent claims of the present application are patented over the cited references. Reconsideration and allowance of the application and presently pending claims 1-13 are respectfully requested.

## CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-13 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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